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10/617,210	07/11/2003	Christian Georg Gerlach	Q76413	3108

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EXAMINER	
WOZNIAK, JAMES S	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/617,210	GERLACH, CHRISTIAN GEORG	
	Examiner	Art Unit	
	JAMES S. WOZNIAK	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,11,13,15-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,11,13,15-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. In response to the office action from 5/23/2008 and the applicant-initiated interview from 8/26/2008, the applicant has submitted an amendment, filed 8/25/2008, and a supplemental amendment, filed 9/29/2008, amending the independent claims 1 and 7, while arguing to traverse the art rejection based on the limitation regarding evaluating the indexes of a codebook as part of determining an optimal codevector *(Supplemental Amendment from 9/29/2008, Page 8)* and the cross-multiplication operation *(Amendment from 8/25/2008, Pages 12-14)*. Applicant's arguments have been fully considered, however the previous rejection is maintained due to the reasons listed below in the response to arguments.

2. In response to amended claims 1 and 7, which incorporate an explanation of the variables included in the cross-multiplication expression, the examiner has withdrawn the previous objection directed to minor informalities.

3. With respect to the 35 U.S.C 112, first paragraph enablement rejection of claim 5, the applicant argues that the examiner has not met the burden of providing reason why the disclosure would not be enabled and further points to portions of the specification in support of the claimed subject matter *(Amendment from 8/25/2008), Pages 10-11)*. In response the examiner notes that the reason of insufficient disclosure with respect to enablement was provided in the previous

Office Action from 5/23/2008 *(Pages 4-5)*. In this portion of the Office Action, it was noted that the reason the specification lacks proper disclosure is because the performing of the various CELP processing functions in parallel is only briefly and generically mentioned. In the specification only a complex vector quantization technique is described in detail, with only a general mention of the CELP functions *(Pages 9-10)*. In other words, it is the application of parallel processing of a DSP to CELP processing including vector coding, which the applicants seem to consider the novelty of the invention *(Specification, Pages 1-2)*. In the case of vector quantization, the applicant has gone into great detail to describe how parallel processors in a DSP are configured to achieve their invention, but in the case of the CELP processing there is no mention of how the DSP may be configured to achieve this aspect of the invention. Would the set-up be similar to the vector quantization process or completely different? The specification does not go into detail on this point because it only generically mentions that the aforementioned processes may be performed in parallel. Further, since this parallel processing is what the applicant seems to consider the novelty of their invention, it should also be described as to how it works with respect to the other CELP processing. Since it only generically mentions parallel processing in passing, the disclosure with respect to claim 5 is insufficient. The cited portions of the applicant's disclosure are not convincing because they lack the aforementioned description and merely replicate the generic statement that is already featured in claim 5. Thus, the applicant's preceding argument has been fully considered, but is not convincing.

4. In response to the cancellation of claim 19, the examiner has withdrawn the previous 35 U.S.C. 112, first paragraph rejection directed to this claim.

5. In response to the clarification of how the equation of claims 1 and 7 is used to determine an optimal codevector and the cancellation of claim 19, the examiner has withdrawn the previous 35 U.S.C. 112, second paragraph rejections.

6. In response to the amended specification, the examiner has withdrawn the previous objection directed towards minor informalities.

Response to Arguments

7. Applicant's arguments have been fully considered but they are not persuasive for the following reasons:

First, the examiner will respond to those arguments presented in the initial amendment filed on 8/25/2008.

With respect to **Claim 1**, the applicant first argues that although Davidson et al *(U.S. Patent: 4,868,867)* teaches a cross-multiplication scheme for a vector search, Davidson does not teach that this search is performed in parallel for every vector and further argues that Kwan et al *("Implementation of DSP-RAM: An Architecture for Parallel Digital Signal Processing in Memory," 2001)* makes no mention of a cross-multiplication scheme *(Amendment from 8/25/2008, Pages 12-14)*. In response, the examiner notes that the Davidson reference is only relied upon to evidence that the cross-multiplication operation recited in the claim 1 is well known in the art for use in optimal vector searching *(Col. 12, Lines 15-59)*. The parallel processing concept is taught by Kwan *(Section 3.3, Pages 344-345)*. Furthermore, Kwan

suggests that different functions can be used to determine an optimal vector *(Sections 3.3, Page 344)*, which would include the searching technique employed by Davidson. Since Davidson describes a clear benefit in using this algorithm *(comparison scheme that is suitable for a DSP that has low memory requirements, Davidson, Col. 12, Lines 52-54)*, one of ordinary skill in the art would have been motivated to combine the cross multiplication algorithm of Davidson with the parallel-processor DSP vector search taught by Kwan. Thus, because it is the combination of Kwan and Davidson that teaches the aforementioned claim limitation, the applicant's arguments have been fully considered, but are not convincing. In response to these arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Next, the applicant argues that it would not have been obvious to combine the teachings of Kwan and Davidson because: a.) Kwan performs searching using an L2 norm and Davidson uses an altogether different technique, b.) cross-multiplication is not even mentioned/required in Kwan, and c.) the inclusion of the cross-multiplication of Davidson in Kwan's vector search would cause it to deviate form its primary purpose of searching codebooks using an L2 norm *(Amendment from 8/25/2008, Pages 14-15)*.

In response to argument a.), the examiner notes that although Kwan does disclose performing vector searching using an L2 norm, there is nothing in Kwan that prevents or eliminates the possibility of using another type of vector search. In fact, Kwan notes that there are alternative types of searching that may be utilized in the art *(Section 3.3, Page 344)*.

Davidson's cross-multiplication-based search is one such method that provides a clear benefit of being suitable for a DSP and having low memory requirements *(Col. 12, Lines 52-54)*. Since Kwan notes other vector search algorithms and Davidson present one that one of ordinary skill in the art would recognize as being beneficial, particularly for use in a DSP as taught by Kwan *(abstract; and Fig. 6)*, this argument has been fully considered, but is not convincing.

In response to argument b.), the examiner notes that cross-multiplication is not required to be recited/required by Kwan in order to incorporate such in algorithm into its system. Instead, it is the benefit of the algorithm which, as noted above and described in Davidson, would motivate one of ordinary skill in the art to modify the teachings of Kwan accordingly. Thus, this argument has been fully considered, but is not convincing.

In response to argument c.), the examiner notes that the primary purpose of Kwan is not performing a vector search using an L2 norm as is alleged by the application. Instead, the primary purpose of the Kwan reference is to perform a vector search in parallel using a DSP to increase the speed of the search *("the increased speed of parallel codebook searching could be a significant advantage", abstract; and Section 3.3, Page 345)*. Davidson's cross-multiplication operation would fall in line with the goal of Kwan because using the cross-multiplication algorithm is efficient/appropriate for use in a DSP and requires little memory, and thus, would achieve a more efficient DSP processor having low memory requirements. The operation of Davison would thus not be altered because only the algorithm would be incorporated into the parallel vector search scheme taught by Kwan to achieve a clear benefit. Thus, this argument has been fully considered, but is not convincing.

The art rejection of claim 7 is traversed for reasons similar to claim 1 *(Amendment from 8/25/2008, Page 15)*. In regards to such arguments, see the above response directed to claim 1.

With respect to further dependent **claim 20**, the applicant argues that Kwan does not disclose anything about evaluating an index and completely fails to disclose anything about evaluating indexes for ensuring conformity with a linear search method *(Amendment from 8/25/2008, Pages 15-16)*. In response, the examiner notes that the index of a codebook represents a vector position in a codebook. Thus, when Kwan performs evaluation for an optimal codevector, the process comprises analysis at each codevector position in a codebook, and thus, analysis of each corresponding vector index *(Pages 344-345)*. In this way, Kwan does teach evaluating indexes in a codebook. Also, in Kwan each codevector index is analyzed in sequence within each processor *(i.e., a linear fashion)*, similar to a non-parallel processor implementation *(Section 3.3, Pages 344-345)*. Finally, the limitation "for ensuring conformity" is an intended outcome for performing index calculation. Although Kwan does teach this limitation, as is pointed out above, the only assocaited structure/step with such an intended outcome is evaulating an index. Since Kwan teaches such index evaluation for the preceding reasons, such a result would flow naturally from such an evaluation because in the claim that step is the only structure/step required for acheiving this intended result. Thus, for at least these reasons, the applicant's arguments have been fully considered, but are not convincing.

The further dependent claims are traversed for reasons similar to independent claims 1 and 7 *(Amendment from 8/25/2008, Page 15)*. In regards to such arguments, see the above response directed to claims 1 and 7.

The examiner will now address those arguments presented in the supplemental amendment filed on 9/29/2008.

With respect to Claim 1, the applicant argues that Kwan fails to teach evaluating indexes in a codebook *(Amendment from 9/29/2008, Page)*. These arguments are similar to those presented above with respect to claim 20. Thus, in regards to such arguments, see the response directed to claim 20. Also, it is further noted that claim 1 does not include any mention of ensuring conformity and claim 20 only requires an index evaluation to ensure conformity *(as is pointed out above)*.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. **Claim 5** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 5 recites performing various CELP processing functions in parallel, however, the specification does not sufficiently describe such parallel processing. More specifically, the specification only describes a complex vector quantization technique implemented in a parallel processor in detail and merely makes a general mention that parallel processing can be applied to the other CELP functions *(Pages 9-10)*. This

general mention of parallel processing does not specifically explain how the various CELP coding processes would be performed in parallel *(as is the case with vector quantization)*, and thus, the specification would not enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention recited in claim 5.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claims 1, 3, 5-9, 11, 13, 15-18, and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al *("Implementation of DSP-RAM: An Architecture for Parallel Digital Signal Processing in Memory," 2001)* in view of Davidson et al *(U.S. Patent: 4,868,867)*.

With respect to **Claim 1**, Kwan recites:

K code vectors is provided for vector quantization of a signal vector representing a set of signal values of said audio or speech signal *(codeword vectors corresponding to a speech signal, Section 3.3, Page 344)*,

Performing a codebook search for determining an optimal code vector of said codebook, wherein said codebook search is performed in parallel by *(codebook search performed in parallel, Section 3.3, Pages 344-345)*:

Dividing the codebook into a plurality of codebook groups *(distributing a voice codebook over multiple processing elements, Section 3.3, Pages 344-345; and Fig. 6)*;

Simultaneously determining a plurality of optimal group code vector each of which corresponds to one of said plurality of codebook groups *(simultaneously determining a lowest error vector match with each divided codevector set, Section 3.3, Pages 344-345)*; and

Determining an optimal code vector of said codebook from the plurality of optimal group code vectors *(finding the closest matching codevector over all of the processing elements, Section 3.3, Pages 344-345)*; and

Outputting the code vector *(sending optimal code vectors, Section 3.3, Page 344)*,

Wherein said determining of said optimal code vector among said plurality of optimal group code vectors comprises evaluating an index of each optimal group code vector uniquely identifying each optimal group code vector within said codebook *(speech vectors having a defining index at which the vector is located, Section 3.3, Page 344, which is analyzed to access the corresponding optimal vector for each group to determine/calculate the overall best codevector, Section 3.3, Pages 344-345)*.

Although Kwan notes that several different error functions can be used to determine an optimal vector *(Section 3.3, Page 344)*, Kwan does not explicitly teach the use of a cross-multiplication expression as a means for vector selection. Such an expression, however, is well known in the speech coding art as is evidenced by Davidson (*Col. 12, Lines 15-59)*.

Kwan and Davidson are analogous art because they are from a similar field of endeavor in speech coding. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to modify the teachings of Kwan with the cross-multiplication expression

taught by Davidson in order to provide a comparison scheme that is suitable for a DSP that has low memory requirements *(Davidson, Col. 12, Lines 52-54)*.

With respect to **Claim 3**, Kwan recites the parallel process for encoding a voice signal as applied to Claim 1. Although Kwan does not explicitly describe the entire encoding process in detail, including a shape-gain step, such a step is well known in the speech coding art as is evidenced by Davidson *(Col. 16, Lines 32-56)*.

Kwan and Davidson are analogous art because they are from a similar field of endeavor in speech coding. Thus, it would have been obvious to a person of ordinary skill in the art, at the time of invention, to modify the teachings of Kwan with the well known gain factor taught by Davidson in order to provide information required for speech synthesis at a decoder that also minimizes distortion in a reproduced speech signal *(Kwan, Col. 3, Lines 7-18)*.

With respect to **Claim 5**, Kwan discloses full implementation of a CELP coder/decoder and explains parallel processing for an aspect of the full process *(Sections 3.3-4, Pages 344-345)*, while Davidson further discloses well-known CELP processing means including a synthesizing section and stored auto-correlation/impulse response matricies *(Col. 12, Line 60- Col. 13, Line 19; Col. 14, Lines 15-56; and Fig. 5)*.

With respect to **Claim 6**, Kwan further discloses:

The codebook comprises pulse code vectors *(CELP codevectors, which comprise excitation pulse vectors, Section 3.3, Page 345)*.

With respect to **Claim 7**, Kwan teaches the method of claim 1 and further discloses:

A processor with configurable hardware and/or with acceleration means specifically designed for said method is used for parallel execution of steps of said method *(digital signal*

processor (configurable hardware) with parallel processing elements (i.e., acceleration means) for faster codebook searching (acceleration means), Fig. 6).

With respect to **Claim 8**, Kwan further discloses:

The processor provides means for simultaneously accessing a plurality of said signal values located in a memory *(simultaneously accessing many stored code vectors in parallel processing elements, Section 3.3, Pages 344-345).*

With respect to **Claim 9**, Kwan further discloses:

A standard processor further comprising a calculation module, is used for parallel execution of steps of said method, and wherein said steps of said method are optimized regarding calculation means of said standard processor and/or execution time *(DSP programmed calculation means used to enable parallel speech coding with increased speed and efficiency, Section 3.3 and 4, Pages 344-345).*

With respect to **Claim 11**, Kwan further discloses:

Coder and decoder, in particular speech and/or audio signal CODEC, capable of performing a method according to claim 1 *(voice coding and decoding, Section 3.3 and 4, Pages 344-345).*

With respect to **Claim 13**, Kwan further discloses:

The processor is a digital signal processor *(DSP, Sections 3.3 and 4, Pages 344-345).*

With respect to **Claim 15**, Kwan further discloses:

A plurality of calculation units, each of which determines optimal code group vectors of a respective one of the plurality of codebook groups, wherein the plurality of calculation unit

execute said determining simultaneously *(plurality of parallel processing elements that each determine a best match within each codevector set, Section 3.3, Page 345 and Fig. 6)*.

With respect to **Claim 16**, Kwan further discloses:

Each codebook group comprises a number of code vectors wherein the number of code vectors is a fraction of the plurality of code vectors (codebook is divided into smaller codevector sets, Fig. 6).

With respect to **Claim 17**, Kwan further discloses:

Each code vector is uniquely identifiable by a unique index *(code vectors are each assigned an index, Section 3.3, Page 344)*.

With respect to **Claim 18**, Kwan further discloses:

The code vectors contained in a first codebook group are mutually exclusive from the code vectors contained in a second codebook group *(different codebook sets are assigned to each processing element to increase searching speech, Fig. 6; and Section 3.3, Page 345)*.

With respect to **Claim 20**, Kwan further discloses:

Evaluating an index of each optimal group code vector ensures conformity with a linear search method *(evaluation of different codeword indexes in a vector search conforms to the coding search standards used in a typical linear search, Section 3.3, Page 344)*.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James S. Wozniak whose telephone number is (571) 272-7632. The examiner can normally be reached on M-Th, 7:30-5:00, F, 7:30-4, Off Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Edouard can be reached at (571) 272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/James S. Wozniak/
Patent Examiner, Art Unit 2626